

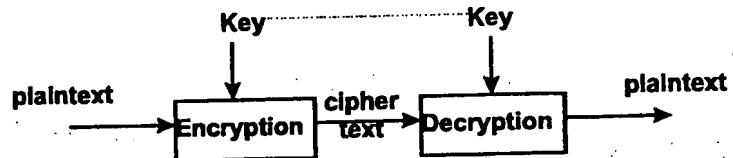
FIGURE 1

四庫全書

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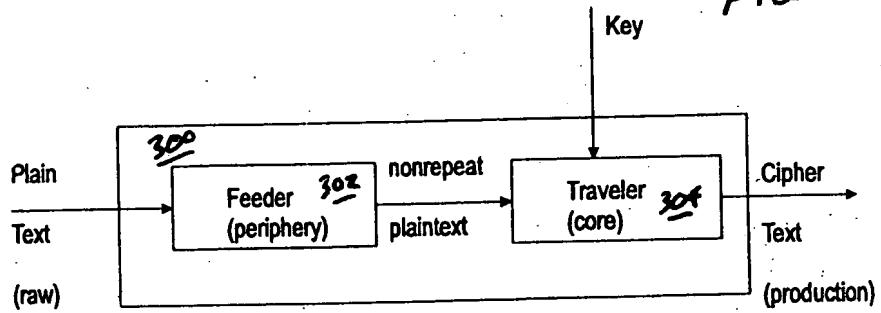
## Daniel Nominal Cycle

FIG. 2



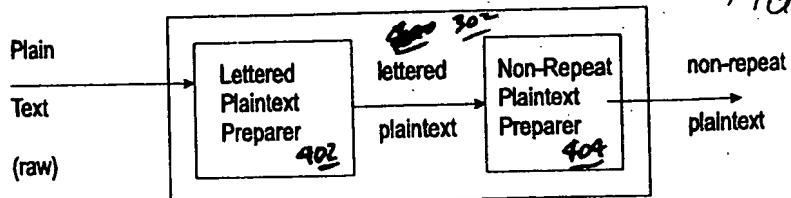
## Daniel Encryption

FIG. 3



## Feeder Module (encryption)

FIG. 4



## Traveler (Core)

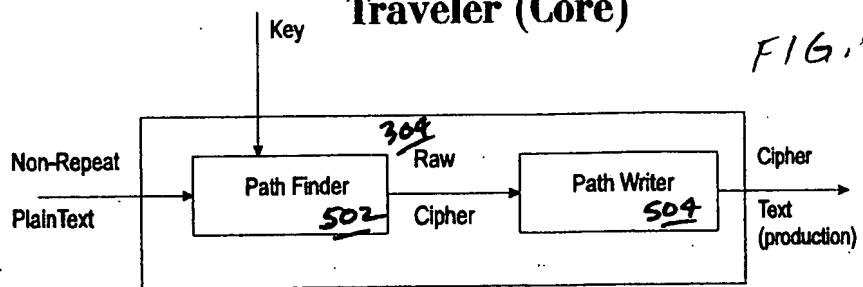


FIG. 5

## Path Finder (Core)

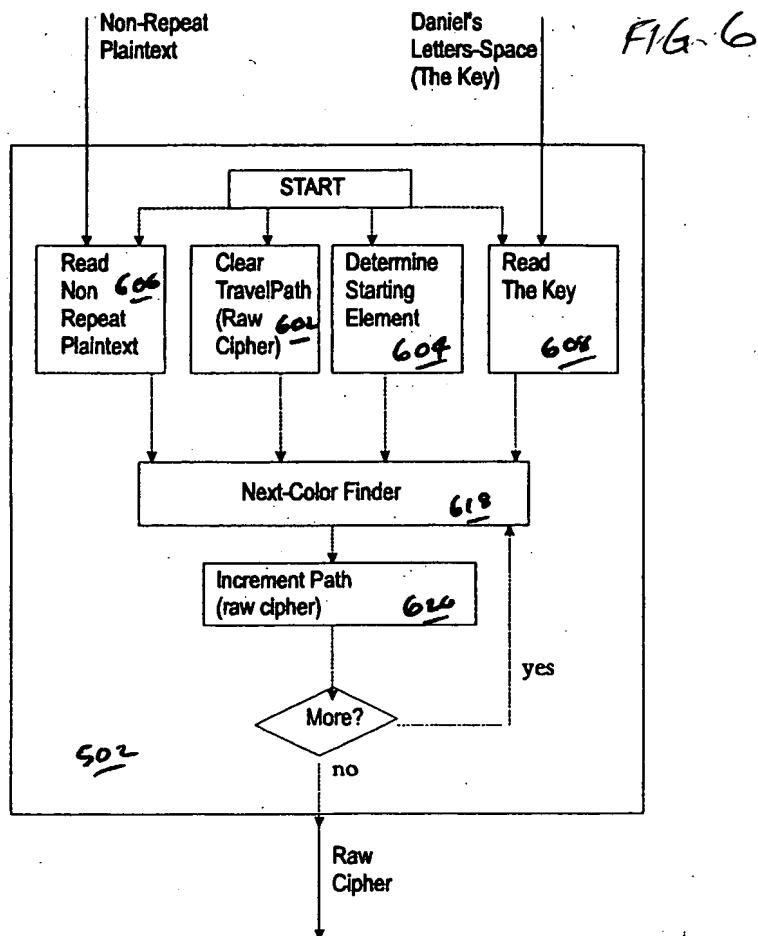


FIG. 6

## Path Finder (Core)

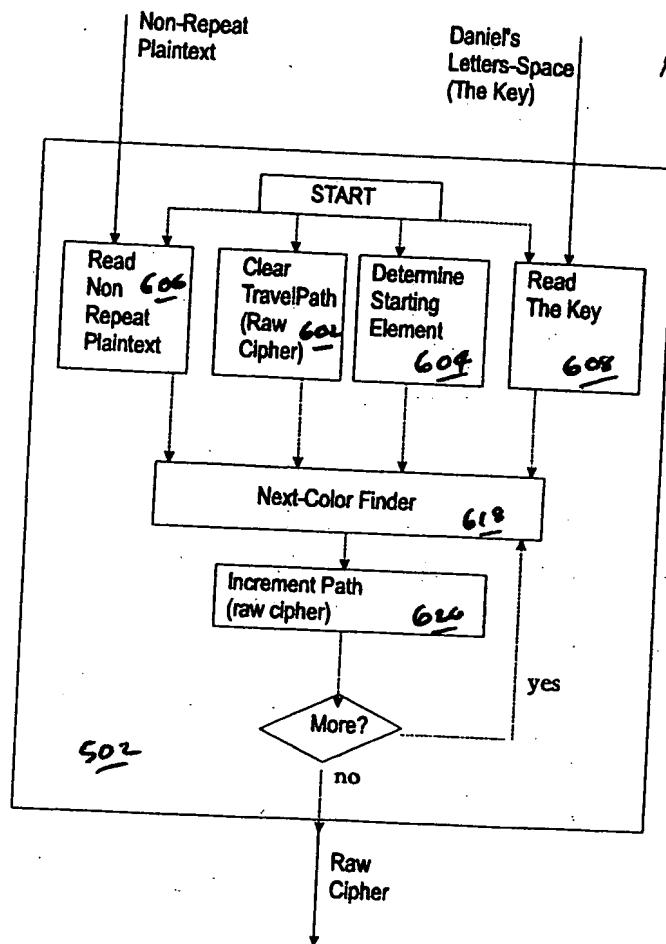
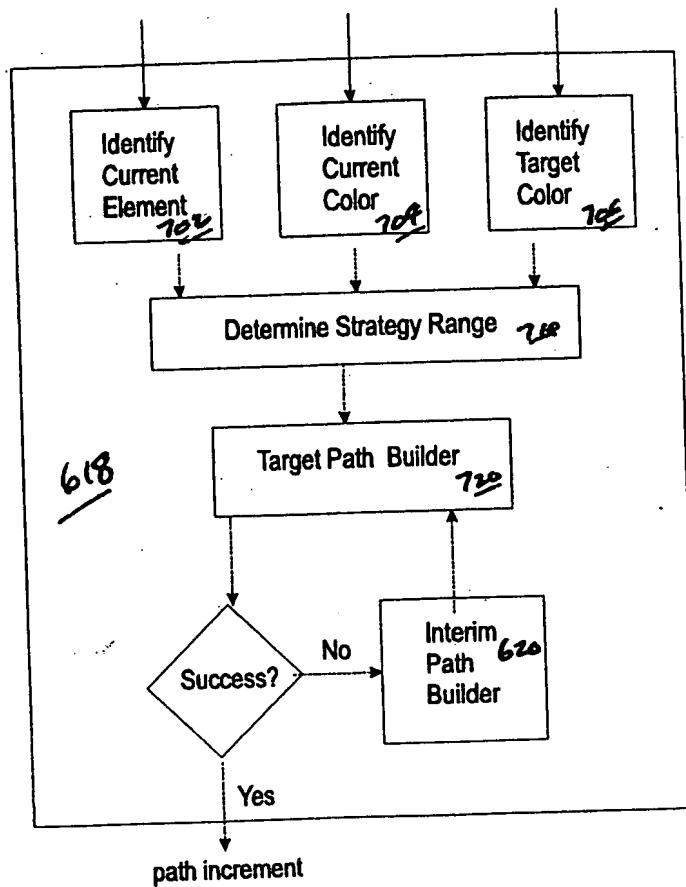


FIG. 6

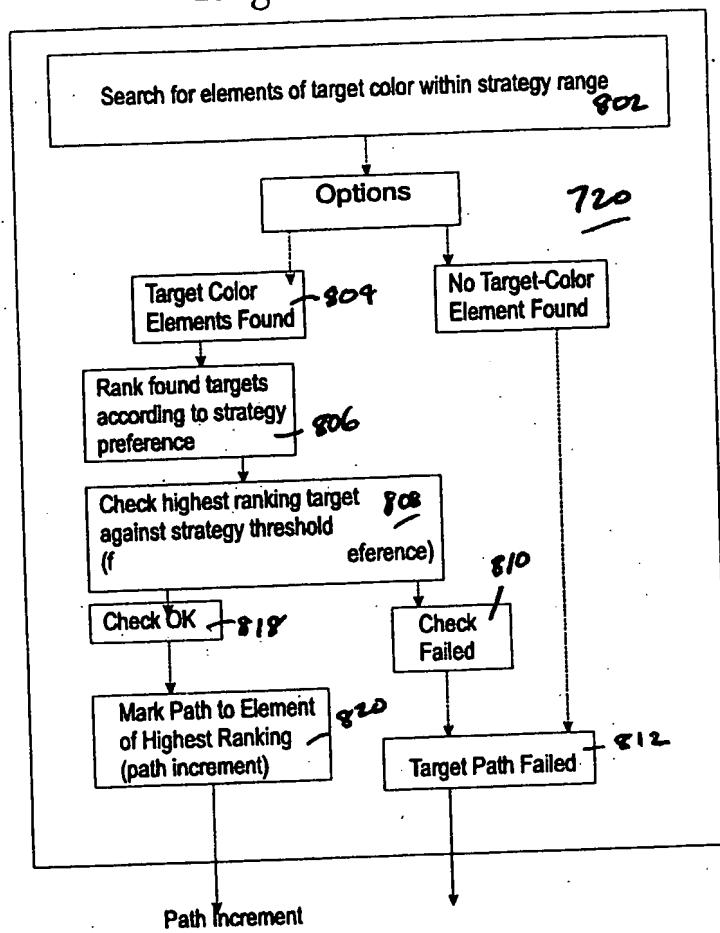
## Next Color Finder

FIG. 7



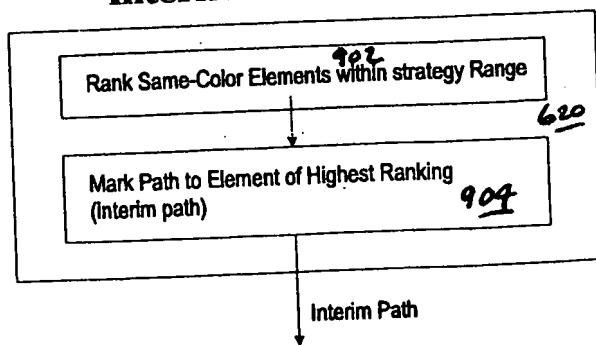
## Target Path Builder

FIG. 8

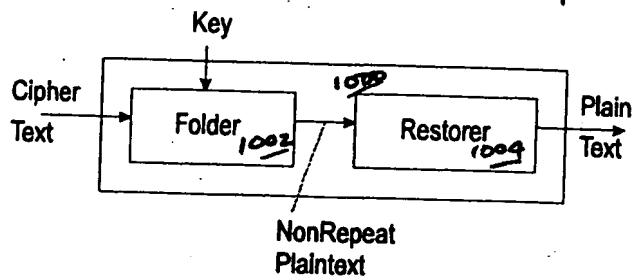


## Interim Path Builder

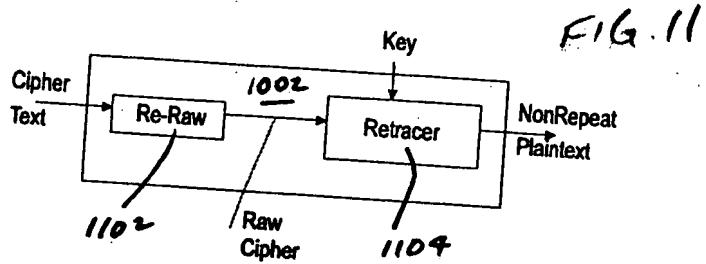
FIG. 9



## Daniel Decryption *FIG. 10*



## The Folder (Core) *FIG. 11*



## Daniel Deniability Configuration

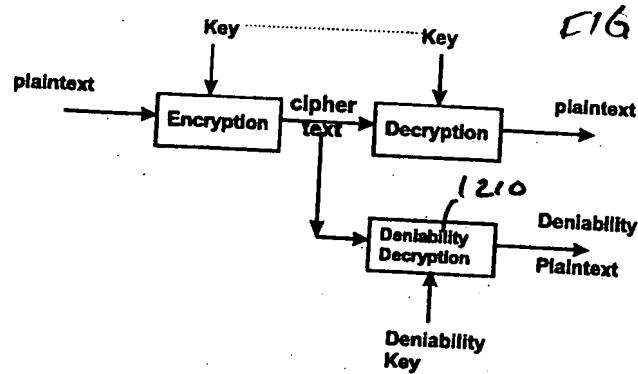


Fig. 12

## Deniability Preparation

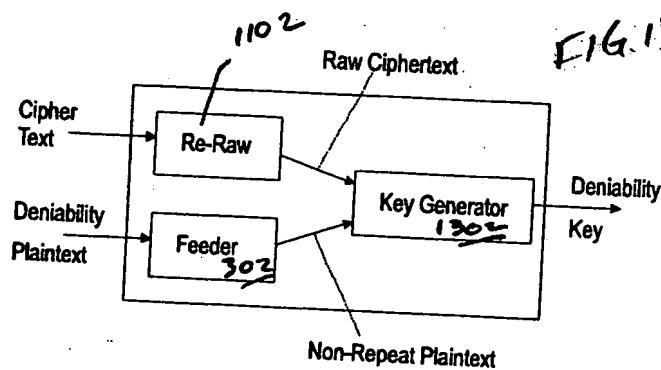


Fig. 13

## The Key Generator

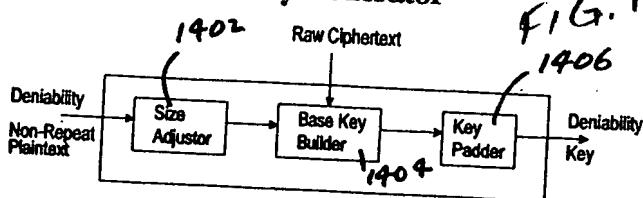


Fig. 14

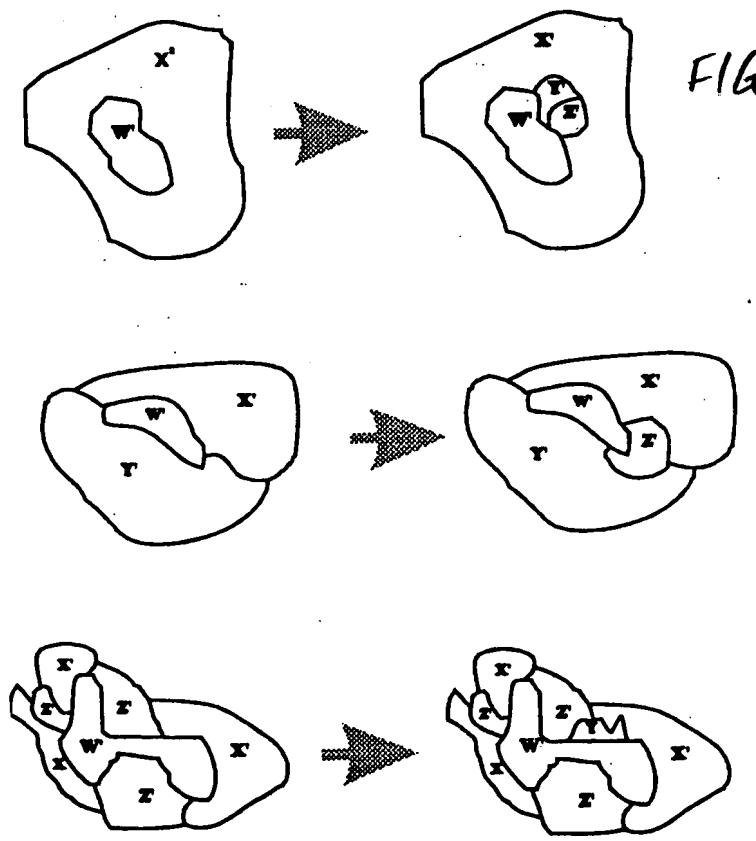
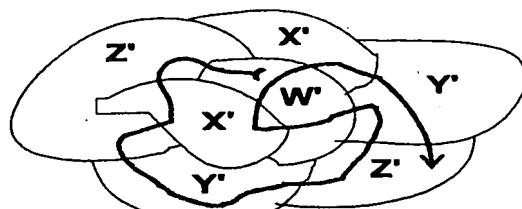


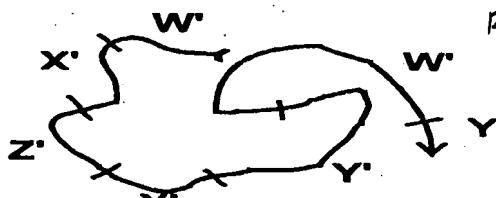
FIG. 15

FIG.16



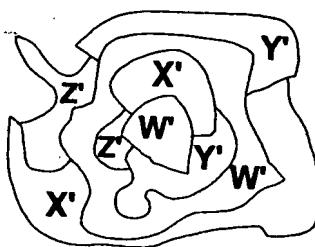
The trail corresponds to the sequence:  
W' Z' X' Z' Y' Z' Y' W' W' X' W' X' Y'.....>

FIG.17



Mapping a sequence of choice  
W' X' Z' X' Y' W' Y'  
On a given cipher.

FIG.18



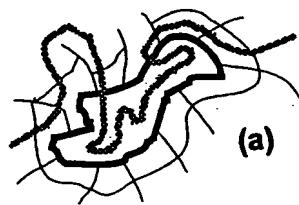
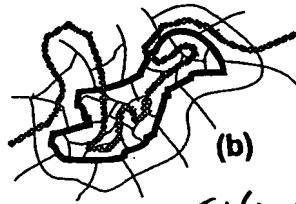


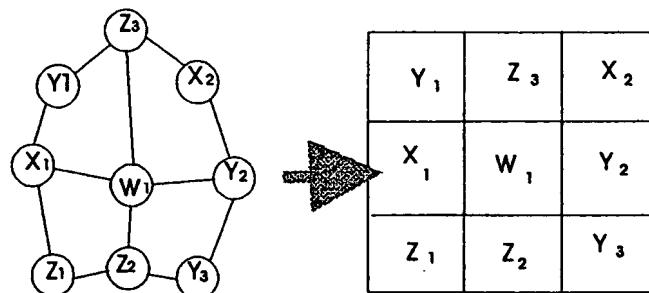
FIG 19 (a)

fig-5



(b)

FIG. 19(b)



Equivalence between arc-represented graph  
and adjacency representation.

FIG. 20

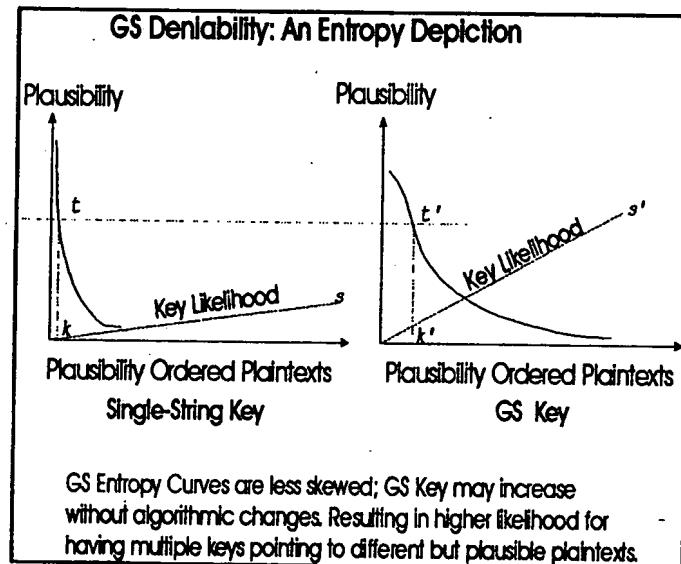


FIG. 21

### gse-gsr configuration

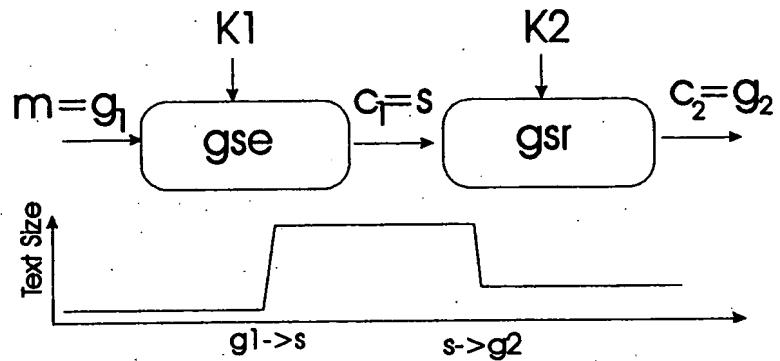


Fig 2-5

FIG. 22

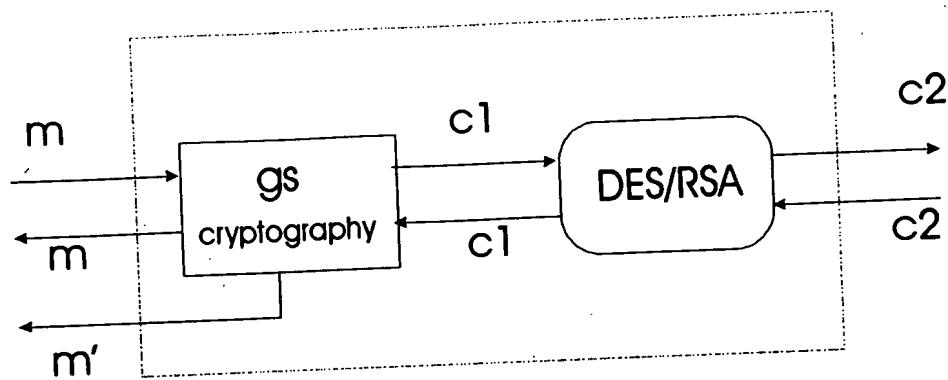


FIG. 23

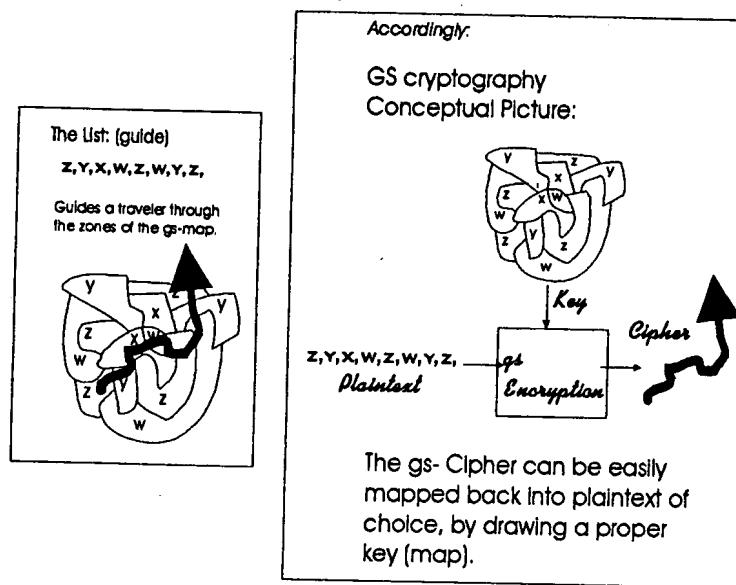


FIG. 24